(REV 10-96)

Rec'd PCT/PTO 17 MAR 1999

ATTORNEY'S DOCKET NUMBER
500.36904X00
FILED: March 17, 1999

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

U.S. APPLICATION NO. (If known, see 37 CFR 1.5)
09/254939

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP97/03267	September 16, 1997	September 17, 1996

TITLE OF INVENTION SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

APPLICANT(S) FOR DO/EO/US Hideo MIURA, Makoto KITANO, Shuji IKEDA, Norio SUZUKI

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [XX] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [ ] This is a **SECOND or SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. [ ] This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. [ ] A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. [X] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [ ] is transmitted herewith (required only if not transmitted by the International Bureau).
   b. [X] has been transmitted by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [XX] A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. [ ] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are transmitted herewith (required only if not transmitted by the International Bureau).
   b. [ ] have been transmitted by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [ ] have not been made and will not be made.
8. [ ] A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. [XX] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. [ ] A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern document(s) or information included:

11. [ ] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [XX] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [XX] A FIRST preliminary amendment.
    [ ] A SECOND or SUBSEQUENT preliminary amendment.
14. [ ] A substitute specification.
15. [XX] A change of power of attorney and/or address letter.
16. [XX] Other items or information:

** International Preliminary Examination Report w/English translation
** International Publication NO. WO98/12742-cover sheet
** Information Disclosure Statement Under 37 CFR 1.97 & 1.98 With Attached References
** Figures 1A-1D,2A-2N,3,4A-4N,5,6A-6N,7,8A-8N,9

6. Application No.	International Application No. PCT/JP97/03267	Attorney's Docket No. 500.36904X00

17. [X] The following fees are submitted:	CALCULATIONS PTO USE ONLY
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):	
Search Report has been prepared by the EPO or JPO ..... $ 840.00	840.00
International preliminary examination fee paid to USPTO (37 CFR 1.482) ..... $ 670.00	
No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) ..... $ 490.00	
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO ..... $ 700.00	
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) ..... $ 96.00	

ENTER APPROPRIATE BASIC FEE AMOUNT =				$ 840.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).				$	
CLAIMS	NUMBER FILED		NUMBER EXTRA	RATE	
Total claims	8	- 20 =		X 18.00	$
Independent claims	7	- 3 =	4	X 78.00	$ 312.00
MULTIPLE DEPENDENT CLAIM(S) (if applicable)				+ 260.00	$
TOTAL OF ABOVE CALCULATIONS =					$ 1,152.00
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also by filed (Note 37 CFR 1.9, 1.27, 1.28).					$
SUBTOTAL =					$ 1,152.00
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +					$
TOTAL NATIONAL FEE =					$ 1,152.00
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40.00 per property +					$ 40.00
TOTAL FEES ENCLOSED =					$ 1,192.00
				Amount to be: refunded	$
				charged	$

a. [X] A check in the amount of $ 1,192.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. [X] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 01-2135. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209

SIGNATURE:

Gregory E. Montone
NAME

28,141
REGISTRATION NUMBER

500.36904X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: H. MIURA et al.

Serial No.: Not Yet Assigned

Filed: March 17, 1999

For: SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

March 17, 1999

Sir:

Prior to examination, please amend the above-identified application as follows:

IN THE CLAIMS

Please add the following new claim:

-- 9. A method of fabricating a semiconductor device comprising the steps of:

(a) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate,

(b) forming trench regions in said substrate from said circuit formation surface thereof,

(c) performing a first oxidation to form an oxide film on said trench regions formed in step (b), and

(d) forming an insulating film inside said oxidized trench regions so as to completely fill them,

characterized by a further step of:

(e) performing a second oxidation to selectively oxidize an opening side of said completely filled trench regions in said substrate. --

REMARKS

Entry of this amendment prior to examination is respectfully requested.

By the present amendment, new claim 9 is added for examination.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of, either by telephone discussion or by personal interview, the Examiner is invited to contact applicants' undersigned attorney at the number indicated below.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (500.36904X00), and please credit any excess fees to said deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

Gregory E. Montone
Registration No. 28,141

GEM/vlc
(703) 312-6600

DESCRIPTION

SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

TECHNICAL FIELD

This invention relates to a semiconductor device having a trench isolation structure having high reliability, and a method of fabricating the same.

BACKGROUND ART

A LOCOS (Local Oxidation of Silicon) structure is known as a structure for electrically insulating and isolating adjacent devices on a semiconductor substrate. This structure is formed by selectively oxidizing a substrate surface to form a thick thermal oxide film, and has been employed in various semiconductor devices. However, because this LOCOS structure has low processing accuracy, it is not suitable for an insulation/isolation structure of high integration semiconductor devices such as deep submicron devices in which high processing dimensional accuracy is required for the thermal oxide film. Therefore, a so-called "trench isolation structure" by a selective oxidation method, which forms shallow trenches in the substrate surface and then selectively oxidizes the trench portions to form the thermal oxide film, has been employed in place of the LOCOS structure as the insulation/isolation structure of

semiconductor devices for which high integration density is required, as described in JP-A-63-143835, for example.

In comparison with the LOCOS structure, this trench isolation structure has the advantage that it can form device isolation oxide films having smaller planar dimensions. For this reason, this method is suitable for the fabrication of deep submicron devices for which processing dimensional accuracy of 0.5 um or below is required.

When a silicon thermal oxide film is formed by oxidizing the surface of a silicon substrate as a semiconductor substrate, for example, a large mechanical stress develops near the interface between the thermal oxide film so formed and the silicon substrate. This is because a part of the silicon substrate (Si) is oxidized and undergoes volume expansion of about twice when it changes to the thermal oxide film (SiO_2). When this mechanical stress increases, crystal defects such as dislocation and stacking faults are likely to occur and reliability of the semiconductor devices drops. It has been also clarified that the oxidation reaction itself (diffusion behavior of oxidizing species, reactivity on the oxidation interface, etc) is affected by the stress and the shape of the growing oxide film changes. Since the stress occurs concentratedly near the end points (corner points) of the two-dimensional or three-dimensional shape, careful attention must be paid

particularly to the crystal defects and the shape change in this stress concentration field.

Figs. 1A to 1D are schematic views of a fabrication process of a trench isolation structure in a conventional selective oxidation method. According to the conventional method shown in Fig. 1A, an oxidation prevention film 3 is first deposited to a surface of a silicon substrate 1 through a pad oxide film (silicon thermal oxide film) 2, then the oxidation prevention film 3, the pad oxide film 2 and the silicon substrate 1 of the area, where a device isolation oxide film is desired to be formed, are partially removed to form a trench (Fig. 1B), and the silicon thermal oxide film 5 is formed by oxidizing the trench surface.

Thereafter, a gate oxide film 6, a gate electrode 7, an inter-layer insulating film 8, a buried insulating film 9, a first layer wiring 10 and a second layer inter-layer insulating film 11 are serially formed.

In this trench isolation structure, the end points (corner points) essentially exist near the trench upper end portion or the trench lower end portion of the substrate. Therefore, the stress concentration field is formed near the end point (corner point) due to thermal oxidation. Because such a stress concentration field is formed, the shape of the substrate, particularly near the trench upper end portion, is oxidized in some cases into a pointed shape 4 having an acute angle as shown in

Fig. 1C. After the formation of the device isolation oxide film, an electronic circuit such as transistors, capacitors, etc, is formed in a device formation area covered with the oxide protective film 3 as shown in Fig. 1D. If such an acute angle portion 4 remains on the substrate surface, however, the concentration of electric field occurs at this portion during the circuit operation and deteriorates the breakdown voltage characteristics of the transistors, the capacitances, etc, that constitutes the circuit, as pointed out by A. Bryant et al. in "Technical Digest of IEDM '94", pp. 671-674.

DISCLOSURE OF INVENTION

In semiconductor devices having a trench isolation structure, the present invention is directed to provide a semiconductor device which does not invite deterioration of breakdown voltage characteristics of transistors and capacitances constituting a circuit but has high reliability, and a method of fabricating such a semiconductor device.

The object described above can be accomplished by preventing a substrate shape in the proximity of the upper end portion of a device isolation trench on a surface of a semiconductor substrate from becoming an acute angle.

A method of fabricating a semiconductor device for accomplishing the object described above includes the following steps.

(1) Step to form oxide prevention film on circuit formation surface of semiconductor substrate:

A silicon substrate, etc, may be used as the semiconductor substrate.

The film thickness of the oxidation prevention film must be such that all the oxide prevention films are not oxidized in the oxidation steps of the post-steps (4), (7), etc.

A polycrystalline silicon thin film, a silicon nitride film, etc, may be used as the oxidation prevention film. Since easily oxidizable materials such as the polycrystalline silicon thin film have low restriction force to volume expansion of the new grown silicon oxide film from the silicon substrate with oxidation, the stress concentration at the trench upper end portion can be reduced. Since difficultly oxidizable materials such as the silicon nitride film have a small oxidation quantity in the oxidation process, the film thickness can be reduced.

It is also effective to form a pad oxide film on the silicon substrate before the oxidation prevention film is formed. If the pad oxide film exists, the portions in the proximity of the lower end of the oxidation prevention film and the upper end of the semiconductor substrate that keep contact with the pad

oxide film are sequentially oxidized from the trench end portion, and the so-called "bird's beak" is formed at the contact portion between the pad oxide film and the semiconductor substrate. As a result, the radius of curvature at the corners near the upper end of the semiconductor substrate is promoted.

(2) Step to form trench having predetermined depth at desired positions of circuit formation surface of semiconductor substrate:

This trench can be formed by an ordinary lithography method using a photoresist and etching, for example.

(3) Step to remove corners formed by trench on circuit formation surface of semiconductor substrate:

This step is not always necessary, but if the corners are removed by this step, the oxidation step (7) of the post-step becomes unnecessary in most cases.

(4) Step to oxidize trench portion formed in semiconductor substrate:

The trench portion is oxidized by several to dozens of nm by oxidation. Due to this oxidation, the bird's beak is grown at the trench portion and a radius of curvature is formed at the corners at the trench upper end portion.

(5) Step to bury buried insulating film into oxidized trench:

Preferably, the material used as the buried insulating film is essentially an insulating material

and has a low dielectric constant. For, if a material having a high dielectric constant is used, a coupling capacitance which is formed when a wiring material is deposited on this insulating film at a post-step becomes great. From this aspect, a silicon oxide film, etc, is a preferred burying material, and polycrystalline silicon or the like is not preferred.

(6) Step to remove buried insulating film formed on oxidation prevention film:

The buried insulating film is etched back by chemical-mechanical polishing (CMP) or dry etching. In this case, the oxidation prevention film serves as an etching stopper and has also the function of preventing etching of the semiconductor substrate below the oxidation prevention film.

(7) Step to oxidize semiconductor substrate after removal of buried insulating film formed on oxidation prevention film:

This step grows the radius of curvature of the trench upper end portion of the semiconductor substrate to a sufficient radius of curvature for preventing the increase of the leakage current. This oxidation step provides also the effect that the buried insulating film is made compact.

This step is not necessary if the radius of curvature at the trench upper end portion of the semiconductor substrate has become sufficient to prevent

the increase of the leakage current due to the oxidation step (4).

This step may be executed before the step (6) or the next step (8). When this step is executed after the next step (8), the surface of the semiconductor substrate is simultaneously oxidized, too, but the oxide film formed on the surface of the semiconductor substrate is removed after completion of additional oxidation and in this way, the step of forming the device isolation oxide film is completed.

(8) Step to remove oxidation prevention film formed on circuit formation surface of semiconductor substrate:

The formation step of the device isolation oxide film is completed by this step. Therefore, a semiconductor device is formed by forming a circuit such as transistors on the semiconductor substrate on which the device isolation oxide film is formed.

A semiconductor device according to the present invention for accomplishing the afore-mentioned objects is a semiconductor device having a device isolation oxide film which is formed on a circuit formation surface of a semiconductor substrate and is a trench isolation structure, wherein an angle θ between the circuit formation surface of the semiconductor substrate and the side surface of the semiconductor substrate in a depth-wise direction of the trench constituting the trench isolation structure is within

the range of $90° < \theta < 180°$. Because this structure can prevent field concentration at the trench upper end portion, it can prevent the increase of a leakage current resulting from deterioration of withstand voltage characteristics of the circuit such as transistors and capacitances formed on the semiconductor substrate.

The coupling capacitance of wirings constituted on the semiconductor substrate can be reduced by burying the inside of the trench by an insulating material having a low dielectric constant such as a silicon oxide, and reliability of the semiconductor device can be further improved.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A, 1B, 1C and 1D are schematic views, each showing a fabrication process of a trench isolation structure in a selective oxidation method according to the prior art;

Figs. 2A to 2N are schematic views, each showing a fabrication process of an MOS transistor according to the first embodiment of the present invention;

Fig. 3 is a flowchart showing the fabrication process of the MOS transistor according to the first embodiment of the present invention;

Figs. 4A to 4N are schematic views, each showing a fabrication process of an MOS transistor according to the second embodiment of the present invention;

Fig. 5 is a flowchart showing the fabrication process of the MOS transistor according to the second embodiment of the present invention;

Figs. 6A to 6N are schematic views, each showing a fabrication process of an MOS transistor according to the third embodiment of the present invention;

Fig. 7 is a flowchart of the fabrication process of the MOS transistor according to the third embodiment of the present invention;

Figs. 8A to 8N are schematic views, each showing a fabrication process of an MOS transistor according to the fourth embodiment of the present invention; and

Fig. 9 is a flowchart of the fabrication process of the MOS transistor according to the fourth embodiment of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

Hereinafter, preferred embodiments of the present invention will be explained with reference to the accompanying drawings.

A fabrication process of an MOS transistor according to the first embodiment of the present invention will be explained with reference to Figs. 2A to 2N and Fig. 3. Figs. 2A to 2N are schematic views of the fabrication process of the MOS transistor according to the first embodiment, and Fig. 3 is a flowchart of the fabrication process of this MOS transistor.

The fabrication process of the MOS transistor of this first embodiment is as follows.

(1) A surface of a silicon substrate 1 is thermally oxidized so as to form a pad oxide film 2 having a thickness of 10 to several tens of nm [Fig. 2B and Fig. 3 (101) to (102)].

(2) A polycrystalline silicon thin film 18 is deposited on the pad oxide film 2 to a thickness of about 10 to 200 nm [Fig. 2B, Fig. (103)]. This polycrystalline silicon thin film 18 is used as an oxidation prevention film when a device isolation thermal oxide film 5 is formed. Incidentally, the polycrystalline silicon film 18 may be directly deposited on the silicon substrate 1 by omitting the formation of the pad oxide film 2.

Incidentally, the following description is based on the assumption that the pad oxide film 2 is formed. Therefore, the process step relating to the pad oxide film 2 is not necessary when the formation of the pad oxide film 2 is omitted.

(3) A photoresist 19 is formed on the polycrystalline silicon film 18 [Fig. 2B, Fig. 3 (104)].

(4) After the photoresist 19 in an area, in which a device isolation film is to be formed, is removed by an ordinary lithography method, a part of each of the polycrystalline silicon thin film 18, the pad oxide film 2 and the silicon substrate 1 is removed by anisotropic etching so as to form a shallow trench whose sidewalls

have a predetermined angle (substantially, about 60 to about 90 degrees) on the surface of the silicon substrate 1 [Figs. 2C to 2D, Fig. 3 (105) to (107)].

(5) After the remaining photoresist 19 is completely removed, thermal oxide is carried out so as to form an oxide film 5 by oxidizing the trench portion formed in the surface of the silicon substrate 1 to several to dozens of nm [Figs. 2E and 2F, Fig. 3 (108) to (109)]. Incidentally, a sufficient film thickness of the polycrystalline silicon thin film 18 deposited as the oxidation prevention film must be secured so that it can function as the oxidation prevention film for preventing the surface side of the polysilicon thin film 18 from being fully oxidized at the time of thermal oxidation and preventing the silicon substrate 1 below this polycrystalline silicon thin film 18 from being oxidized entirely. When this pad oxide film 2 exists, silicon in the proximity of the lower end of the polycrystalline silicon thin film 18 and the upper end of the silicon substrate 1 keeping contact with the pad oxide film 2 is sequentially oxidized from the trench end, and a so-called "bird's beak" is formed between the contact portions. As a result, the radius of curvature in the proximity of the upper end of the silicon substrate 1 is promoted. From this aspect, the pad oxide film 2 is preferably formed.

(6) Because the inside of the trench is not completely buried by this trench oxidation, an

insulating film 9 such as a silicon oxide film is deposited by chemical vapor deposition, sputtering, etc, in order to completely bury the inside of the trench covered by the thermal oxidation film (hereinafter, the insulating film 9 for burying the inside of the trench will be called the "buried insulating film 9") [Fig. 2G, Fig. 3 (110)]. Basically, the material used for this buried insulating film 9 is an insulating material and preferably has a low dielectric constant. For, when a material having a high dielectric constant is used, a coupling capacitance formed when a wiring material is deposited on this film in a post-step becomes greater. From this aspect, it is not preferred to use polycrystalline silicon as the burying material.

(7) The buried insulating film 9 is then etched back by chemical-mechanical polishing (CMP) or dry etching [Fig. 2G, Fig. 3 (111)]. In this case, the polycrystalline silicon thin film 18 used as the oxidation prevention film functions as an etching stopper and plays the role of preventing the silicon substrate 1 below the polycrystalline silicon thin film 18 from being etched.

(8) When the radius of curvature of the trench upper end portion 12 due to the bird's beak grown between the contact portions by the oxidation of the trench portion of the silicon substrate 1 is sufficient for preventing the increase of the leakage current, the formation step of the device isolation oxide film is

completed by removing the polycrystalline silicon thin film 18 and the pad oxide film 2 [Fig. 2H, Fig. 3 (113)].

When the radius of curvature of the trench upper end portion 12 due to the bird's beak grown by the oxidation of the trench portion of the silicon substrate 1 is not sufficient for preventing the leakage current depending on the product specification for each product, for example, thermal oxidation is again carried out (hereinafter called "additional oxidation") after the buried insulating film 9 is etched back from the next product lot [Fig. 2I, Fig. 3 (112)].

In this case, since the buried insulating film 9 has already been formed inside the trench of the silicon substrate 1, oxidation proceeds from near the trench upper end portion 12 and the inside of the trench is hardly oxidized for the following reason. In other words, though the inside of the trench is to be thermally oxidized through the buried insulating film 9, a longer time is necessary for the oxidation seeds to diffuse inside the buried insulating film 9 before reaching the silicon substrate 1 than when the silicon substrate is directly oxidized. Therefore, oxidation hardly proceeds substantially within a short period of several minutes near the bottom of the trench. On the other hand, a weak boundary layer of the coupling portion deposited by chemical vapor deposition or sputtering to the trench sidewalls and the upper surface

of the trench exists at the trench upper end portion 12, and the oxidation seeds can diffuse at a relatively high rate along this weak boundary layer. As a result, the oxidation seeds are supplied to the trench upper end portion 12 within a short time (10 or more minutes at the oxidation temperature of 850°C), so that only the portions in the proximity of the trench upper end portion 12 are oxidized preferentially and the formation of the radius of curvature of the trench upper end portion 12 is promoted.

Furthermore, this additional oxidation provides the effect of rendering the buried insulating film 9 compact. After this additional oxidation is completed, the formation step of the device isolation oxide film is completed by removing the polycrystalline silicon thin film 18 and the pad oxide film 2 [Fig. 2M, Fig. 3 (113)].

This additional oxidation may be carried out after the polycrystalline silicon thin film 18 is removed. In this case, the surface of the silicon substrate 1 is simultaneously oxidized, too, but the formation step of the device isolation oxide film is completed by removing this oxide film formed on the surface of the silicon substrate 1 after the additional oxidation is completed.

(9) Transistor structures, etc, are formed on the silicon substrate 1 [Figs. 2J, K, L, N(h), Fig. 3 (114) to (122)].

Conventional fabrication technologies of the transistor structure, etc, can be employed without particular limitation, and a typical fabrication proces of the MOS transistor structure will be explained next by way of example.

(a) Any of a silicon oxide film, a silicon nitride film, an acid nitride film and a high dielectric thin film (insulating films of a higher dielectric constant than SiO_2 such Ta_2O_5, PZT, and BsT), or their laminate body, is formed as the gate oxide film 6 on the silicon substrate 1.

These thin films can be formed by CVD, or the like, for example. The silicon oxide film may be formed by thermal oxidation of the silicon substrate 1.

(b) Any of a polycrystalline silicon thin film, a metal thin film such as a tungsten film and a silicide thin film, or their laminate body, is formed, and then unnecessary portions are removed by etching, etc, to form a gate electrode 7.

(c) An impurity is implanted and a first layer wiring 10, an inter-layer insulating film 11, etc, are formed.

Further, an inter-layer insulating film 14, a wiring 15 and an insulting film 16 are formed, whenever necessary.

The MOS transistor described above can be used for memory circuits such as a DRAM (Dynamic Random

Access Memory) or arithmetic operation circuits such as logic devices.

The first embodiment described above can prevent the acute angle portions from remaining near the trench upper end portions of the silicon substrate when the trench isolation structure is formed as the device isolation oxide film structure, can prevent the increase of the leakage current or the drop of withstand voltage characteristics of the MOS transistor resulting from the field concentration in the proximity of the gate electrode film, by forming the radius portions or the obtuse angle portions near the trench upper end portion of the silicon substrate, and can improve electrical reliability of the transistor.

Incidentally, since the trench upper end portion of the silicon substrate before thermal oxidation is substantially orthogonal in the first embodiment, there is the case where the radius of curvature near the trench upper end portion of the silicon substrate is not sufficient. However, because polycrystalline silicon as the oxidation prevention film is easily oxidized, the restriction force to the volume expansion of the newly grown silicon oxide from the silicon substrate is lower in comparison with those materials which are difficultly oxidized, and there is sometimes the case where additional oxidation is not necessary. Furthermore, processing of the trench is

easy and this embodiment is excellent in the aspect of productivity, too.

Next, the fabrication process of an MOS transistor according to the second embodiment of the present invention will be explained with reference to Figs. 4A to 4N and Fig. 5. Figs. 4A to 4N are schematic views showing the fabrication process of the MOS transistor according to the second embodiment, and Fig. 5 is a flowchart of the fabrication process of the MOS transistor of this embodiment.

The fabrication process of the MOS transistor of the second embodiment modifies the fabrication step (4) of the first embodiment in the following way. Since the fabrication steps other than the step (4) are the same as those of the first embodiment, the detailed explanation will be omitted.

(4) After the photoresist 19 of the area in which the device isolation film is to be formed is removed by an ordinary exposure method, a part of each of the polycrystalline silicon thin film 18, the pad oxide film 2 and the silicon substrate 1 is removed by etching, and a shallow trench is formed in the surface of the silicon substrate 1. When forming the trench in the surface of the silicon substrate, isotropic etching is applied near the trench upper end portion so as to form the radius of curvature near the trench upper end portion, and then anisotropic etching is applied so as to define the trench shape having the slope portion like the isotropic

etching portion 13. Incidentally, the angle of the trench sidewalls near the trench lower end portion need not always be 90 degrees and a predetermined inclination (substantially within the range of 60 to 90 degrees) [Figs. 4C, D, E, Fig. 5 (205) to (207)] may be formed.

In comparison with the second embodiment, the etching step, that is, isotropic etching and anisotropic etching, at the time of formation of the shallow trench becomes more complicated. However, because the isotropic etching portion 13 is disposed at the trench upper end portion of the silicon substrate at the time of formation of the shallow trench as described above, oxidation of the trench upper end portion of the silicon substrate 1 by first thermal oxidation (formation of the radius of curvature) is promoted, and the necessity for additional oxidation becomes lower.

Next, the fabrication process of an MOS transistor according to the third embodiment of the present invention will be explained with reference to Figs. 6A to 6N and Fig. 7. Figs. 6A to 6N are schematic views of the fabrication process of the MOS transistor according to the third embodiment and Fig. 7 is a flowchart of the fabrication process of the MOS transistor of this embodiment.

The fabrication process of the MOS transistor according to the third embodiment is as follows.

(1) The surface of the silicon substrate 1 is thermally oxidized and the pad oxide film 2 having a

thickness of 10 to dozens of nm is formed [Figs. 6B, Fig. 7 (301) to (302)].

(2) A silicon nitride film 17 having high oxidation resistance is deposited to a thickness of 10 to 200 nm on the pad oxide film 2 [Fig. 6B, Fig. 7 (303)]. This silicon nitride film 17 is used as an oxidation prevention film when the device isolation oxide film 5 is formed. Incidentally, the silicon nitride film 17 having high oxidation resistance may be directly formed on the silicon substrate 1 by omitting the formation of the pad oxide film 2. Alternatively, the silicon nitride film 17 is deposited through the pad oxide film 2 and te polycrystalline silicon thin film, or through only the polycrystalline silicon thin film. In either case, the silicon nitride film 17 exists on the outermost surface of the structure.

Incidentally, the following description is based on the assumption that the polycrystalline silicon thin film and the pad oxide film 2 are formed. Therefore, when the formation of the polycrystalline silicon thin film and the pad oxide film 2 is omitted, the process steps relating to the polycrystalline silicon thin film and the pad oxide film 2 are not necessary.

(3) The photoresist 19 is formed on the silicon nitride film 17 [Fig. 6B, Fig. 7 (304)].

(4) After the photoresist 19 of the area in which the device isolation film is to be formed is removed by

an ordinary lithography method, the silicon nitride film 17, the pad oxide film 2 and the polycrystlaline silicon film are removed by etching. Next, the photoresist is removed, and the shallow trench is formed in the surface of the silicon substrate 1 by dry etching. When this trench is formed in the surface of the silicon substrate, isotropic etching is applied to the portions near the trench end portion so as to form the radius of curvature in the proximity of the trench upper end and then anisotropic etching is applied to form the trench shape having the slope portion like the isotropic etching portion 13. Incidentally, the angle of the trench sidewalls near the trench lower end portion need not always be 90 degrees, and a predetermined inclination (substantially within the range of 60 to 90 degrees) may be formed, as well [Figs. 6C, D, E, Fig. 7 (305) to (308)].

(5) After the photoresist 9 is removed, thermal oxidation is carried out to oxidize the trench portion formed in the surface of the silicon substrate 1 to a thickness of several to dozens of nm [Figs. 6E, D, F, Fig. 7 (309)]. Incidentally, the film thickness of the silicon nitride film 17 as the oxidation prevention film must be a film thickness sufficient to function as the oxidation prevention film to prevent the silicon nitride film 17 from being completely oxidized at the time of thermal oxidation and to prevent the silicon substrate 1 below the silicon nitride film 17 from being completely

oxidized. Since this silicon nitride film 17 has high oxidation resistance, the film thickness can be made thinner than the polycrystalline silicon thin film 18 used in the first and second embodiments. When the pad oxide film 2 exists, silicon in the proximity of the upper end portion of the silicon substrate 1 keeping contact with the pad oxide film 2 and the lower end of the polycrystalline thin film are serially oxidized from the trench end, and the so-called "bird's beak" is formed, so that the radius of curvature near the upper end of the silicon substrate 1 is promoted. From this aspect, the pad oxide film 1 is preferably formed.

(6) Since the inside of the trench is not fully buried by this trench oxidation, the insulating film 9 such as a silicon oxide film is deposited to bury the inside of the trench by chemical vapor deposition, sputtering, etc, in order to fully bury the inside of the trench covered by the thermal oxidation film (hereinafter, the insulating film 9 for burying the inside of the trench will be called the "buried insulating film 9") [Fig. 6G, Fig. 7 (310)].

Fundamentally, the material used for the burying insulating film 9 is preferably a material having an insulating property and a low dielectric constant. For, when a material having a high dielectric constant is used, a coupling capacitance formed when a wiring material is deposited on the film material in the post-process becomes great. From this aspect, the use

of polycrystalline silicon as the burying material is not preferred.

(7) When the radius of curvature at the trench upper end portion due to the bird's beak grown by the oxidation of the trench portion of the silicon substrate 1 is sufficient to prevent the increase of the leakage current, the formation process of the device isolation oxide film is completed by etching back the buried insulating film 9 and then removing the remaining silicon nitride film 17, polycrystalline silicon and pad oxide film 2 [Figs. 6H, I, Fig. 7 (313)].

When the radius of curvature of the trench upper end portion due to the bird's beak grown by the oxidation of the trench portion of the silicon substrate 1 is not sufficient for preventing the increase of the leakage current, thermal oxidation is again carried out (hereinafter called "additional oxidation") before the buried insulating film 9 is etched back [Fig. 6L, Fig. 7 (312)].

In this case, since the buried insulating film 9 has already been formed inside the trench of the silicon substrate 1, oxidation proceeds from portions near the trench upper end portion 12 and the inside of the trench is hardly oxidized for the following reason.

In other words, thermal oxidation inside the trench is carried out through the buried insulating film 9 but in this case, a longer time is necessary for the oxidation seeds to diffuse inside the buried insulating

film 9 before reaching the silicon substrate 1 than when the silicon substrate is directly oxidized. Therefore, oxidation does not substantially proceed within a short time of several minutes near the bottom of the trench. On the other hand, a weak boundary layer of the coupling portion of the buried insulating film 9 deposited to the trench sidewalls and the trench upper surface by chemical vapor deposition or sputtering exists at the trench upper end portion 12. Accordingly, the oxidation seeds can diffuse at a relatively high rate along this weak boundary layer, so that the oxidation seeds are supplied to the trench upper end portion 12 within a short time (10 minutes or more at an oxidation temperature of 850°C), the portions near the trench upper end portion 12 are oxidized preferentially and the formation of the radius of curvature of the trench upper end portion 12 is promoted.

When the radius of curvature of the trench upper end portion 12 due to the bird's beak grown by this additional oxidation is sufficient to prevent the increase of the leakage current, the formation process of the device isolation oxide film is completed by etching back the buried insulating film 9 and then removing the remaining silicon nitride film 17, polycrystalline silicon and pad oxide film 2 [Fig. 6M, Fig. 7 (313)].

Incidentally, this additional oxidation need not always be carried out before etch-back of the buried

insulating film 9, and may be carried out after etch-back of the buried insulating film 9 in accordance with the product specification required for products in the same way as in the first embodiment.

(8) A transistor structure, etc, is formed on the silicon substrate 1 [Figs. 6J to 6N, Fig. 7 (314) to (322)].

Conventional fabrication technologies of the transistors can be employed without particular limitation, and the explanation will be given on a typical fabrication process of the MOS transistor structure by way of example.

(a) Any one of a silicon oxide film, a silicon nitride film, an acid nitride film and a high dielectric thin film, or their laminate body, is formed as the gate oxide film 6 on the silicon substrate 1.

These thin films can be formed by CVD, for example. The silicon oxide film may be formed by the thermal oxidation of the silicon substrate 1.

(b) After any of a polycrystalline silicon thin film, a metal film such as a tungsten film and a silicide thin film, or their laminate body, is formed, unnecessary portions are removed by etching, etc, to form the gate electrode 7.

(c) An impurity is implanted and a first layer wiring 10, an inter-layer insulating film 11, etc, are formed. Wirings of the second layer et seq, and an insulating film are formed further, whenever necessary.

The MOS transistor described above can be used for memory circuits such as a DRAM (Dynamic Random Access Memory), an SRAM or arithmetic operation circuits such as logic devices (Static Random Access Memory), etc.

In the fabrication process of the MOS transistor, the third embodiment prevents the acute angle portions from remaining in the proximity of the trench upper end portion of the silicon substrate when forming the trench isolation structure as the device isolation oxide film structure but forms the radius of curvature portion or the obtuse angle portion near the trench upper end portion of the silicon substrate. Therefore, this embodiment can prevent the increase of the leakage current of the MOS transistor or the drop of the breakdown voltage characteristics resulting from the field concentration near the end portion of the gate electrode, and can improve electrical reliability of the transistor.

Incidentally, since the third embodiment uses the silicon nitride film 17 having high oxidation resistance as the oxidation prevention film, the film thickness of the oxidation prevention film can be reduced, and removal of this oxidation prevention film in the final process step becomes easier.

The etching process at the time of the formation of the shallow trench gets complicated in this third embodiment in the same way as in the second

embodiment, but because the isotropic etching portion 13 is disposed at the trench upper end portion of the silicon substrate 1 when the shallow trench is formed as described above, oxidation of the trench upper end portion of the silicon substrate 1 is promoted in the initial thermal oxidation process and the necessity for additional oxidation becomes lower.

Next, the fabrication process of an MOS transistor according to the fourth embodiment of the present invention will be explained with reference to Figs. 8A to 8N and Fig. 9. Figs. 8A to 8N are schematic views of the fabrication process of the MOS transistor of the fourth embodiment and Fig. 9 is a flowchart of the fabrication process of the MOS transistor in this embodiment.

The fabrication process of the MOS transistor of the fourth embodiment modifies the fabrication step (4) of the first embodiment in the following way. Since the fabrication steps other than the step (4) are the same as those of the first embodiment, the detailed explanation will be omitted.

(4) After the photoresist in the area in which the device isolation film is to be formed is removed by an ordinary lighography method, the silicon nitride film 17, the pad oxide film 2 and the polycrystalline silicon thin film are removed by etching. Next, the photoresist is removed and the shallow trench is formed in the surface of the silicon substrate 1 by dry etching. The

angle of the trench sidewalls near the trench lower end portion need not always be 90 degrees and a predetermined inclination (substantially within the range of 760 to 90 degrees) may be formed [Figs. 8C, D, E, Fig. 9 (405) to (408)].

Since the fourth embodiment uses the silicon nitride film 17 having high oxidation resistance as the oxidation prevention film in the same way as in the third embodiment, the film thickness of the oxidation prevention film can be reduced, and removal of the oxidation prevention film in the final process step becomes easier.

The fourth embodiment can easily form the trench by anisotropic etching alone, and has high productivity.

INDUSTRIAL APPLICABILITY

In the semiconductor devices having the trench isolation structure, the embodiments of the present invention can provide a semiconductor device which does not invite deterioration of the transistors constituting the circuit and the breakdown voltage characteristics of the capacitance, and a method of fabricating the semiconductor device.

CLAIMS

1. A method of fabricating a semiconductor device comprising the steps of:

(a) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate;

(b) forming a trench having a desired depth at a predetermined position of the circuit formation surface of said semiconductor substrate;

(c) oxidizing said trench portion formed in said semiconductor substrate;

(d) burying a buried insulating film into said trench so oxidized;

(e) removing said buried insulating film formed on said oxidation prevention film; and

(f) removing said oxidation prevention film formed on the circuit formation surface of said circuit substrate.

2. A method of fabricating a semiconductor device comprising the steps of:

(a) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate;

(b) forming shallow trenches having a radius of curvature at corners in a desired position of the circuit formation surface of said semiconductor substrate;

(c) forming a trench having a predetermined depth to said shallow trenches having a radius of curvature so formed;

(d) oxidizing said trench portions formed in said semiconductor substrate;

(e) burying a buried insulating film into said trenches so oxidized;

(f) removing said buried insulating film formed on said oxidation prevention film; and

(g) removing said oxidation prevention film formed on the circuit formation surface of said semiconductor substrate.

3. A method of fabricating a semiconductor device according to claim 2, wherein said step for forming shallow trenches is carried out by isotropic etching and said step for forming a trenches having a predetermined depth is carried out by anisotropic etching.

4. A method of fabricating a semiconductor device comprising the steps of:

(a) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate;

(b) forming trenches having a predetermined depth at desired positions of the circuit formation surface of said semiconductor substrate;

(c) oxidizing said trench portions formed in said semiconductor substrate;

(d) burying a buried insulating film into said trenches so oxidized;

(e) removing said buried insulating film formed on said oxidation prevention film;

(f) oxidizing said semiconductor substrate

after said buried insulating film formed on said oxidation prevention film is removed; and

(g) removing said oxidation prevention film formed on the circuit formation surface of said semiconductor substrate.

5. A method of fabricating a semiconductor substrate comprising the steps of:

(a) forming an oxidation prevention film on a circuit formation surface of a semiconductor;

(b) forming shallow trenches having a radius of curvature at corners in desired positions of the circuit formation surface of said semiconductor substrate;

(c) forming trenches having a predetermined depth in said shallow trenches having a radius of curvature;

(d) oxidizing said trench portions formed in said semiconductor substrate;

(e) burying a buried insulation film into said trenches so oxidized;

(f) removing said buried insulating film formed on said oxidation prevention film;

(g) oxidizing said semiconductor substrate after said buried insulating film formed on said oxidation prevention film is removed; and

(h) removing said oxidation prevention film formed on the circuit formation surface of said semiconductor substrate.

6. A method of fabricating a semiconductor device according to claim 5, wherein said step for forming shallow trenches is carried out by isotropic etching and said step for forming a trenches having a predetermined depth is carried out by anisotropic etching.

7. A semiconductor device of the type wherein a device isolation oxide film structure formed on a circuit formation surface of a semiconductor substrate is a trench isolation structure, characterized in that an an angle θ of a trench, which constitutes said trench isolation structure with the circuit formation surface of said semiconductor substrate, in a depth-wise direction with respect to the side surface of said semiconductor substrate is within the range of $90° < \theta < 180°$.

8. A semiconductor device of the type wherein a device isolation oxide film structure formed on a circuit formation surface of a semiconductor substrate is a trench isolation structure, characterized in that an angle θ of a trench, which constitutes said trench isolation structure with the circuit formation surface of said semiconductor substrate, in a depth-wise direction with respect to the side surface of said semiconductor substrate is within the range of $90° < \theta < 180°$, and a silicon oxide exists inside said trench.

ABSTRACT

In a semiconductor device having a trench isolation structure, after a trench surface is selectively oxidized by a conventional method, an oxidation prevention film is removed, the entire surface of the substrate is again oxidized while only an oxide film on the substrate or trench surface is exposed, and a radius of curvature is provided to the shape of the oxide film near the trench upper end portion.

FIG. 1A
PRIOR ART

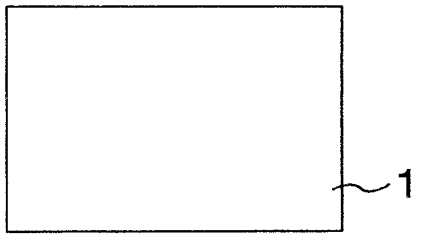


FIG. 1B
PRIOR ART

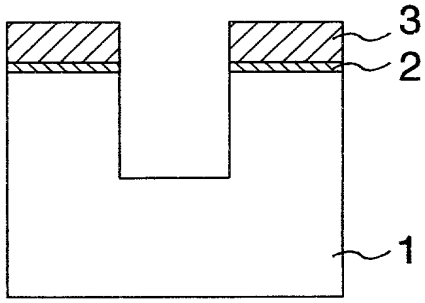


FIG. 1C
PRIOR ART

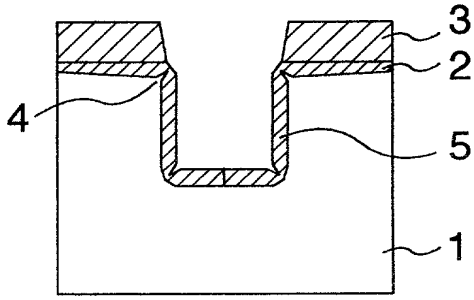


FIG. 1D
PRIOR ART

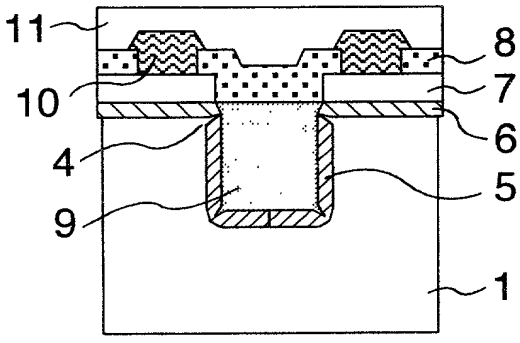


FIG. 2A

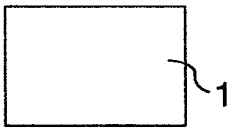


FIG. 2B

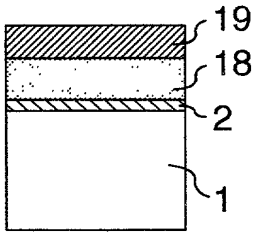


FIG. 2C

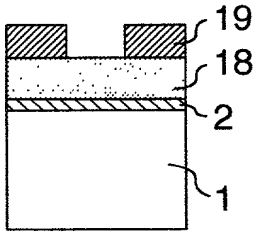


FIG. 2D

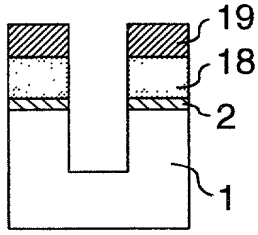


FIG. 2E

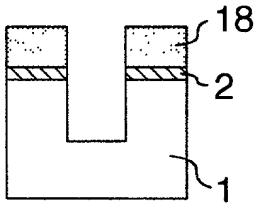


FIG. 2F

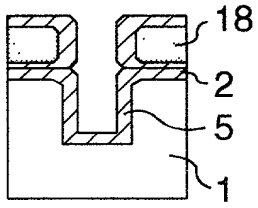


FIG. 2G

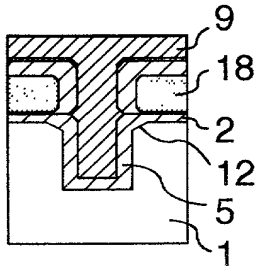


FIG. 2H

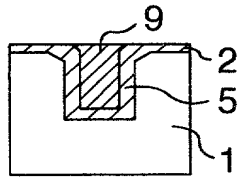


FIG. 2I

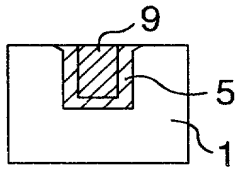


FIG. 2J

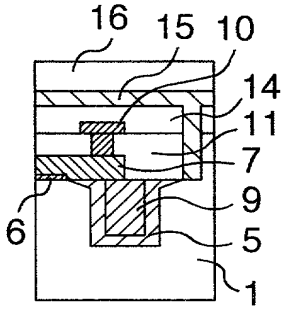


FIG. 2K

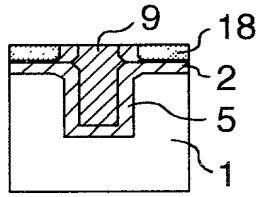


FIG. 2L

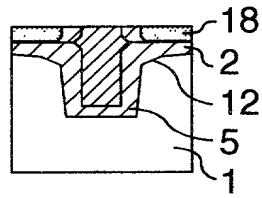


FIG. 2M

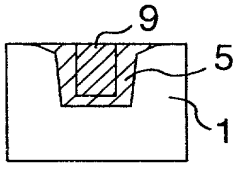


FIG. 2N

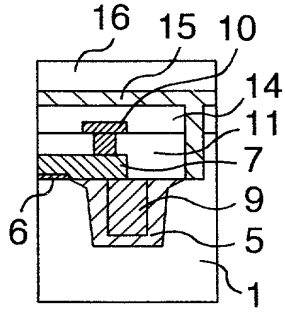


FIG. 3

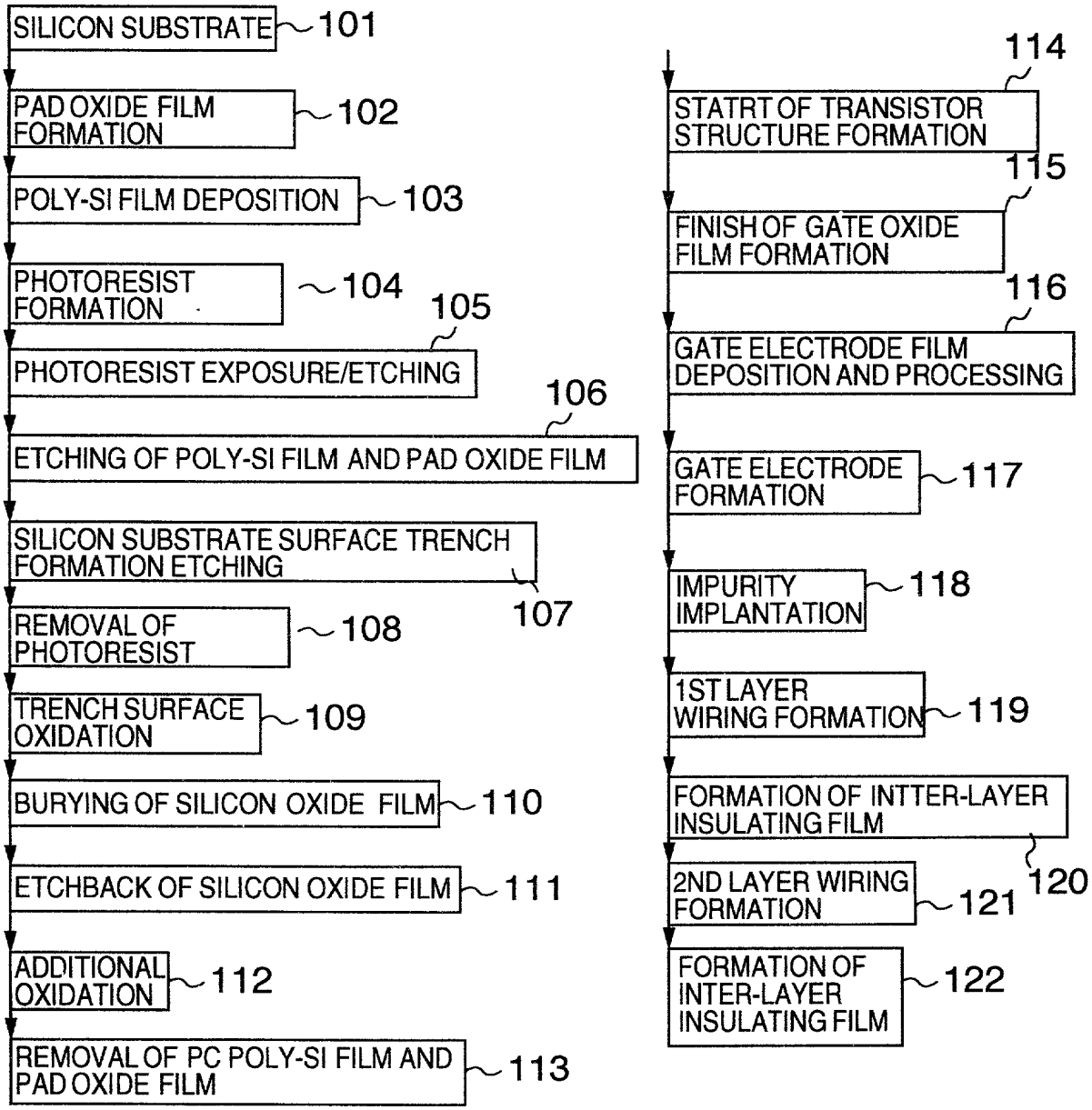

SILICON SUBSTRATE
101
PAD OXIDE FILM FORMATION
102
POLY-SI FILM DEPOSITION
103
PHOTORESIST FORMATION
104
105
PHOTORESIST EXPOSURE/ETCHING
106
ETCHING OF POLY-SI FILM AND PAD OXIDE FILM
SILICON SUBSTRATE SURFACE TRENCH FORMATION ETCHING
107
REMOVAL OF PHOTORESIST
108
TRENCH SURFACE OXIDATION
109
BURYING OF SILICON OXIDE FILM
110
ETCHBACK OF SILICON OXIDE FILM
111
ADDITIONAL OXIDATION
112
REMOVAL OF PC POLY-SI FILM AND PAD OXIDE FILM
113
114
STATRT OF TRANSISTOR STRUCTURE FORMATION
115
FINISH OF GATE OXIDE FILM FORMATION
116
GATE ELECTRODE FILM DEPOSITION AND PROCESSING
GATE ELECTRODE FORMATION
117
IMPURITY IMPLANTATION
118
1ST LAYER WIRING FORMATION
119
FORMATION OF INTTER-LAYER INSULATING FILM
120
2ND LAYER WIRING FORMATION
121
FORMATION OF INTER-LAYER INSULATING FILM
122

FIG. 4A

FIG. 4B

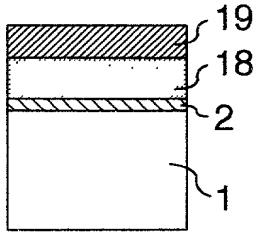


FIG. 4C

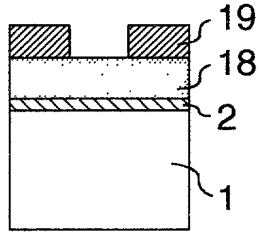


FIG. 4D

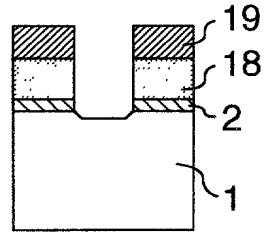


FIG. 4E

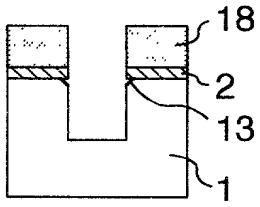


FIG. 4F

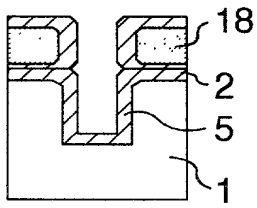


FIG. 4G

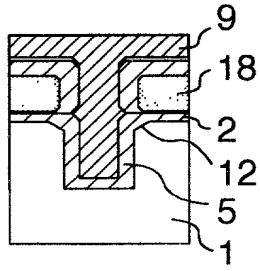


FIG. 4H

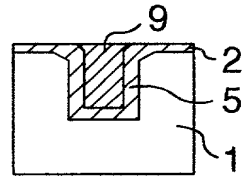


FIG. 4I

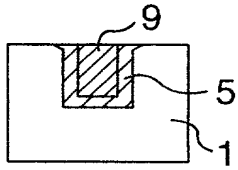


FIG. 4J

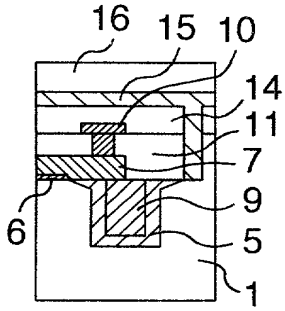


FIG. 4K

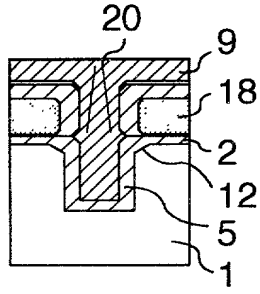


FIG. 4L

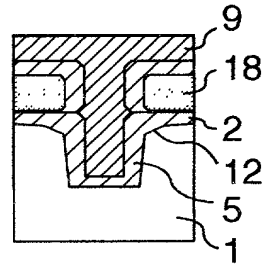


FIG. 4M

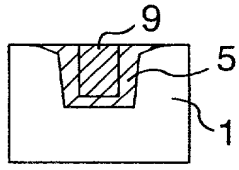


FIG. 4N

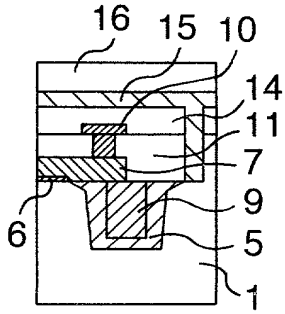


FIG. 5

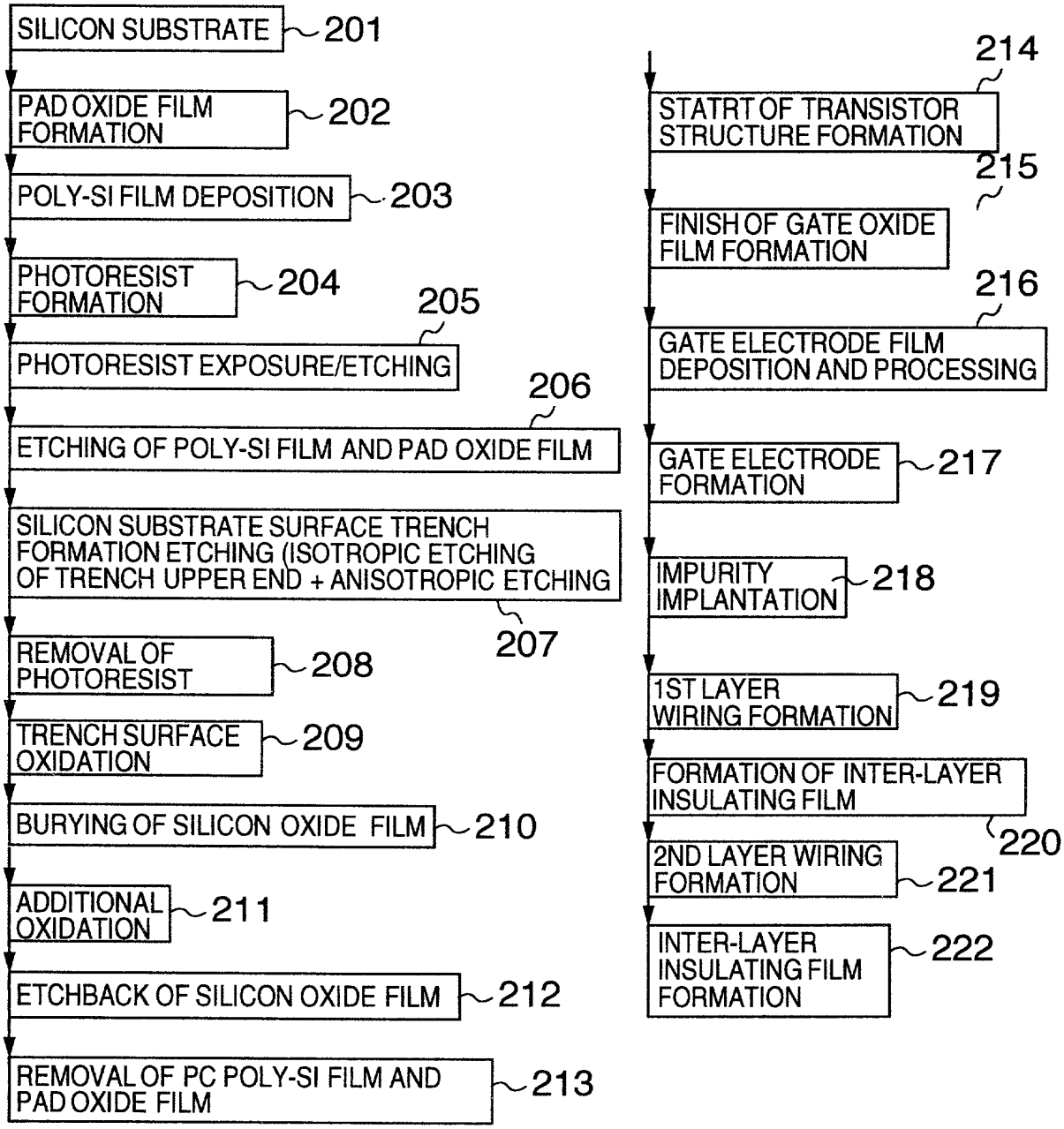

SILICON SUBSTRATE
201
PAD OXIDE FILM FORMATION
202
POLY-SI FILM DEPOSITION
203
PHOTORESIST FORMATION
204
205
PHOTORESIST EXPOSURE/ETCHING
206
ETCHING OF POLY-SI FILM AND PAD OXIDE FILM
SILICON SUBSTRATE SURFACE TRENCH FORMATION ETCHING (ISOTROPIC ETCHING OF TRENCH UPPER END + ANISOTROPIC ETCHING
207
REMOVAL OF PHOTORESIST
208
TRENCH SURFACE OXIDATION
209
BURYING OF SILICON OXIDE FILM
210
ADDITIONAL OXIDATION
211
ETCHBACK OF SILICON OXIDE FILM
212
REMOVAL OF PC POLY-SI FILM AND PAD OXIDE FILM
213
214
STATRT OF TRANSISTOR STRUCTURE FORMATION
215
FINISH OF GATE OXIDE FILM FORMATION
216
GATE ELECTRODE FILM DEPOSITION AND PROCESSING
GATE ELECTRODE FORMATION
217
IMPURITY IMPLANTATION
218
1ST LAYER WIRING FORMATION
219
FORMATION OF INTER-LAYER INSULATING FILM
220
2ND LAYER WIRING FORMATION
221
INTER-LAYER INSULATING FILM FORMATION
222

FIG. 6A

FIG. 6B

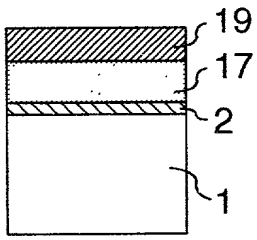


FIG. 6C

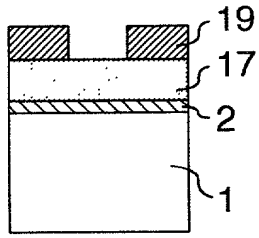


FIG. 6D

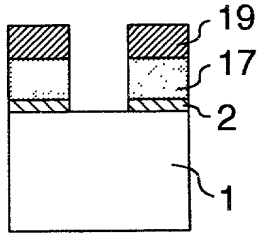


FIG. 6E

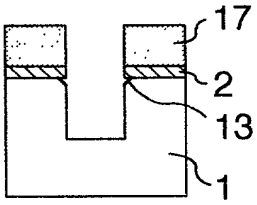


FIG. 6F

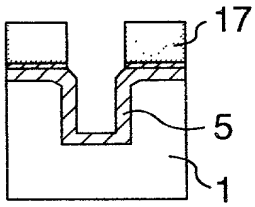


FIG. 6G

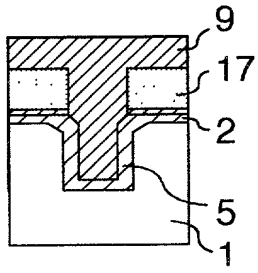


FIG. 6H

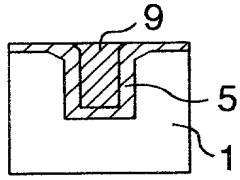


FIG. 6I

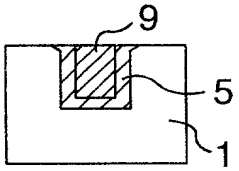


FIG. 6J

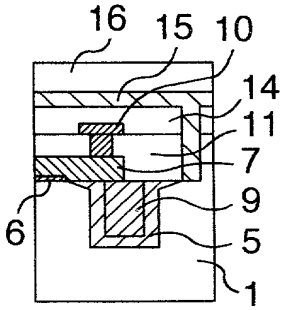


FIG. 6K

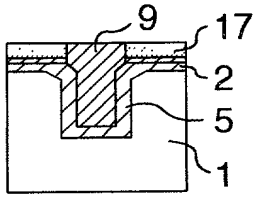


FIG. 6L

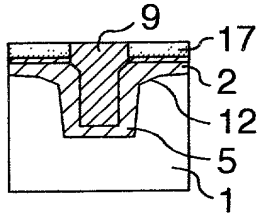


FIG. 6M

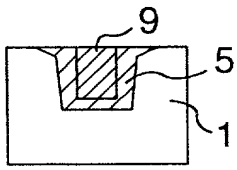


FIG. 6N

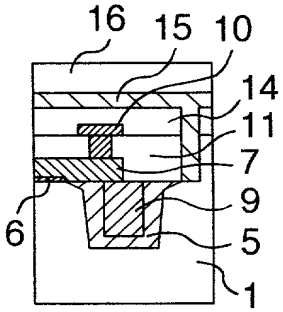


FIG. 7

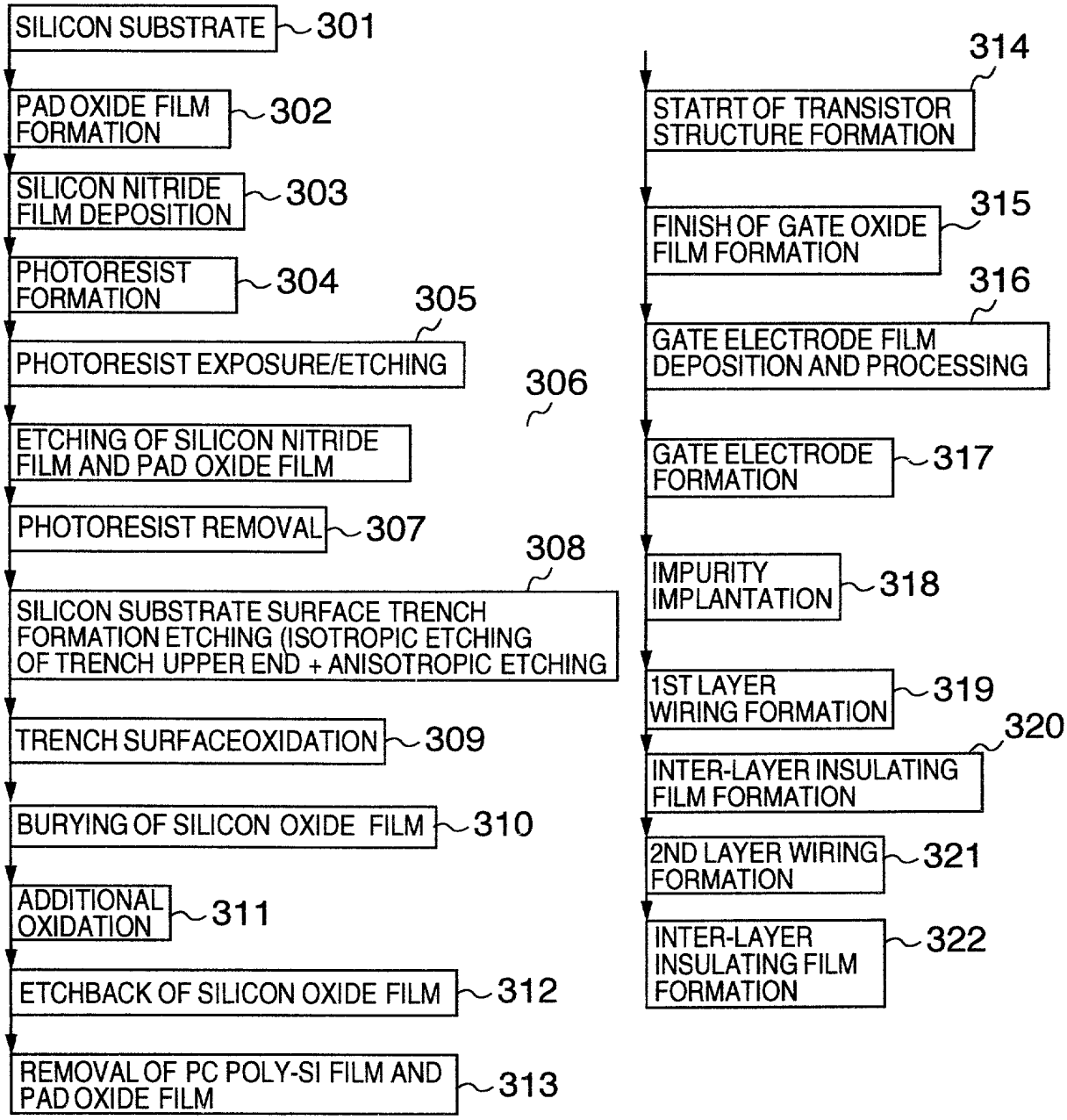

SILICON SUBSTRATE
301
PAD OXIDE FILM FORMATION
302
SILICON NITRIDE FILM DEPOSITION
303
PHOTORESIST FORMATION
304
305
PHOTORESIST EXPOSURE/ETCHING
306
ETCHING OF SILICON NITRIDE FILM AND PAD OXIDE FILM
PHOTORESIST REMOVAL
307
308
SILICON SUBSTRATE SURFACE TRENCH FORMATION ETCHING (ISOTROPIC ETCHING OF TRENCH UPPER END + ANISOTROPIC ETCHING
TRENCH SURFACEOXIDATION
309
BURYING OF SILICON OXIDE FILM
310
ADDITIONAL OXIDATION
311
ETCHBACK OF SILICON OXIDE FILM
312
REMOVAL OF PC POLY-SI FILM AND PAD OXIDE FILM
313
314
STATRT OF TRANSISTOR STRUCTURE FORMATION
315
FINISH OF GATE OXIDE FILM FORMATION
316
GATE ELECTRODE FILM DEPOSITION AND PROCESSING
GATE ELECTRODE FORMATION
317
IMPURITY IMPLANTATION
318
1ST LAYER WIRING FORMATION
319
320
INTER-LAYER INSULATING FILM FORMATION
2ND LAYER WIRING FORMATION
321
INTER-LAYER INSULATING FILM FORMATION
322

FIG. 8A

FIG. 8B

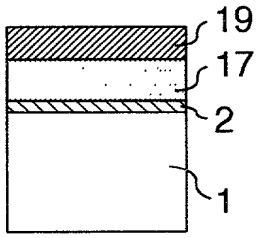


FIG. 8C

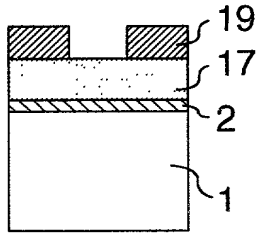


FIG. 8D

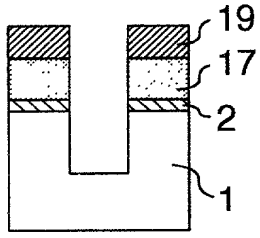


FIG. 8E

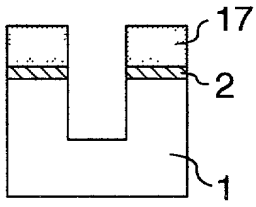


FIG. 8F

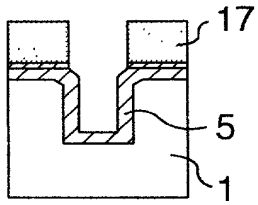


FIG. 8G

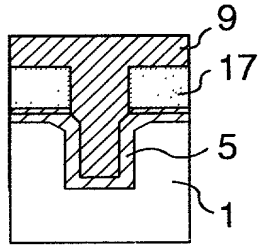


FIG. 8H

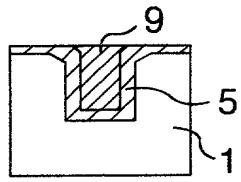


FIG. 8I

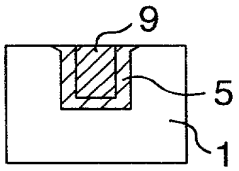


FIG. 8J

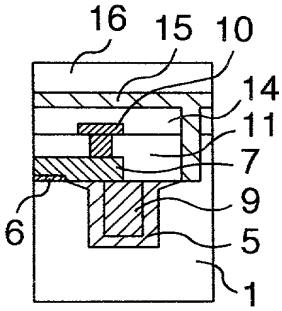


FIG. 8K

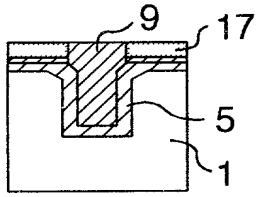


FIG. 8L

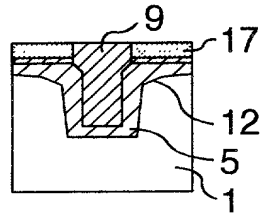


FIG. 8M

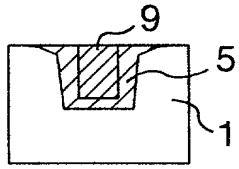


FIG. 8N

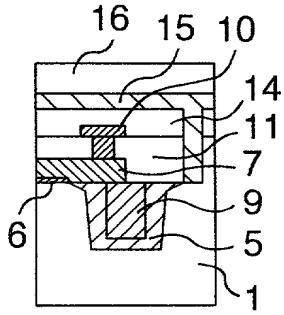
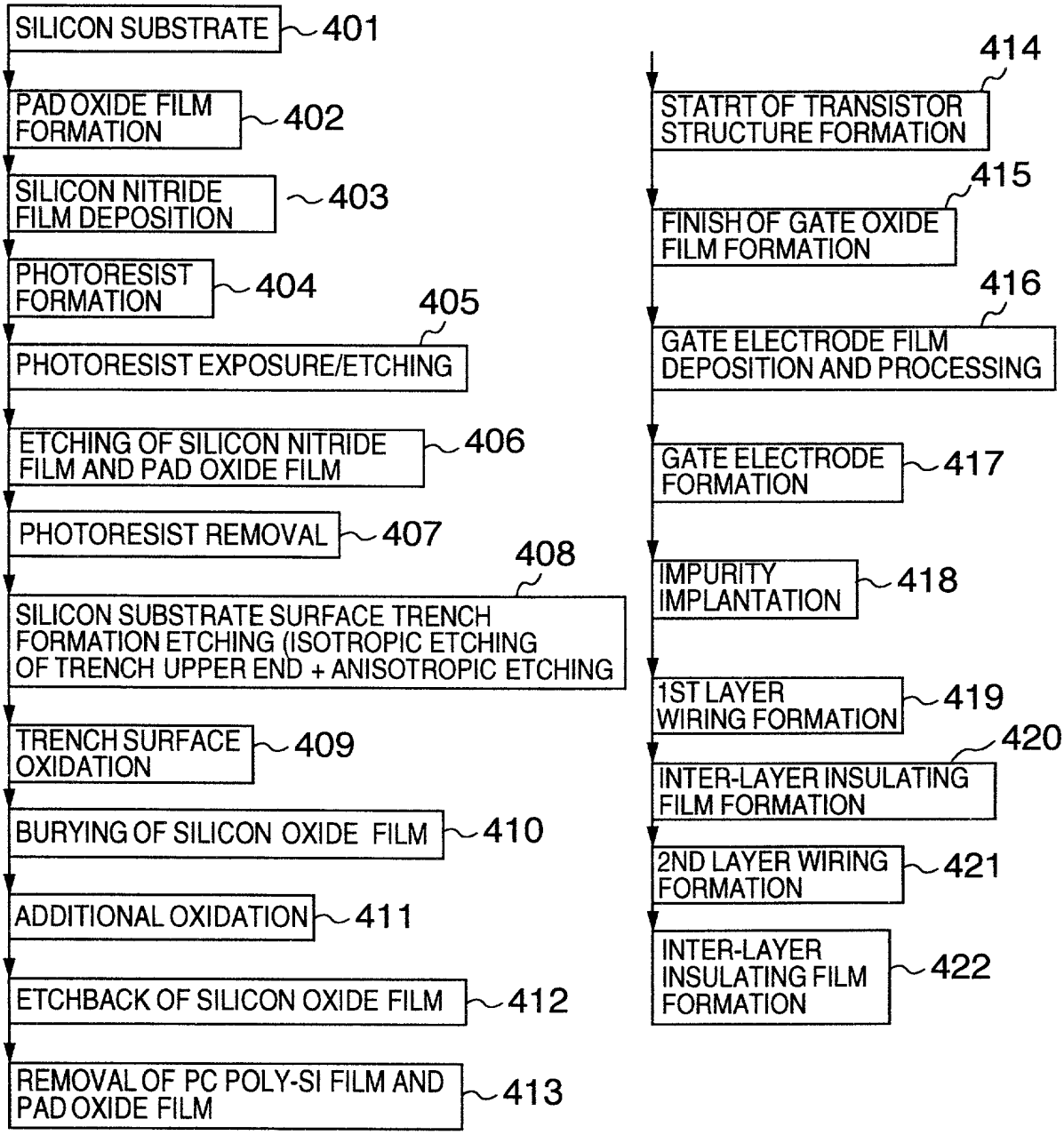


FIG. 9



COMBINED DECLARATION AND POWER OF ATTORNEY
(宣誓書及び委任状)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name, I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

"SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME"

the specification of which: (check one) ☐ is attached hereto.

☒ was filed on September 16, 1997
as Application Serial No. PCT/JP97/03267
and was amended on Nov.19,1998 (PCT Art. 34)
(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended, by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me which is material to patentability in accordance with Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date earlier than that of the application(s) on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
08-244445 (Number)	Japan (Country)	17 Sep., 1996 (Day/Month/Year Filed)	☒ Yes	☐ No
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes	☐ No
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes	☐ No

I hereby claim the benefit under Title 35, United States Code, 120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code § 112, I acknowledge the duty to discolse to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international fiiling date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

(Continued on Page 2)

I hereby appoint as principal attorneys; Donald R. Antonelli, Reg. No. 20,296; David T. Terry, Reg. No. 20,178; Melvin Kraus, Reg. No. 22,466; Stanley A. Wal, Reg. No. 26,432; William I. Solomon, Reg. No. 28,565; Gregory E. Montone, Reg. No. 28,141; Ronald J. Shore, Reg. No. 28,577; Donald E. Stout, Reg. No. 26,422; Alan E. Schiavelli, Reg. No. 32,087 and James N. Dresser, Reg. No. 22,973 to prosecute and transact all business connected with this application and any related United States application and international applications. Please direct all communications to the following address:

Antonelli, Terry, Stout & Kraus
Suite 1800
1300 North Seventeenth Street
Arlington, Virginia 22209
Telephone: (703) 312-6600

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

宣誓日　　発明者フルネームサイン　　氏名タイプ欄

Date Jan. 25, 1999 Inventor Hideo Miura Hideo MIURA

Residence Koshigaya-shi, SAITAMA JAPAN Citizenship Japan

Post Office Address 8-9-512, Minamikoshigaya 4-chome, Koshigaya-shi, SAITAMA 343 JAPAN. JPV

Date Jan. 25, 1999 Inventor Makoto Kitano Makoto KITANO

Residence Tsuchiura-shi, IBARAKI JAPAN Citizenship Japan

Post Office Address 1057-8, Shiratorimachi, Tsuchiura-shi, IBARAKI 300 JAPAN. JPK

Date Jan. 25, 1999 Inventor Shuji Ikeda Shuji IKEDA

Residence Koganei-shi, TOKYO JAPAN Citizenship Japan

Post Office Address 30-8, Nukuikitamachi 3-chome, Koganei-shi, TOKYO 184 JAPAN. JPK

Date Jan. 25, 1999 Inventor Norio Suzuki Norio SUZUKI

Residence Mito-shi, IBARAKI JAPAN Citizenship Japan

Post Office Address 1-1, Atagocho, Mito-shi, IBARAKI 310 JAPAN. JPV

Date _____ Inventor _____

Residence _____ Citizenship _____

Post Office Address _____

Date _____ Inventor _____

Residence _____ Citizenship _____

Post Office Address _____